International Journal on Advanced Science Engineering Information Technology

Vol.14 (2024) No. 6
ISSN: 2088-5334

Power-efficient 4-bit 40-MS/s Time-domain 2-times Interpolating Flash ADC Using Complementary Latching Technique

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***Abstract*—We propose a power-efficient 4-bit 40-MS/s 2-times time-domain interpolating flash analog-to-digital converter (ADC) using complementary dynamic amplifiers (CDAs). The flash ADC can be utilized for high-speed data conversion. However, as the resolution of a conventional flash ADC increases, the number of comparators grows, resulting in greater area and higher power consumption. To address these drawbacks, we propose a comparator structure consisting of one CDA, two types of latches, and a 2-times time-domain interpolation technique using these CDAs. The CDA can amplify twice in one clock cycle, reducing the design burdens such as power consumption, high-speed clock drivers, and high-speed dynamic latches compared to the conventional dynamic amplifier (DA)-based flash ADC. A CDA-based time-domain interpolation technique is also applied to improve power and area efficiencies in the proposed flash ADC. The prototype ADC was fabricated using a 500 nm CMOS process (2-poly, 3-metal). Thanks to the power-efficient CDA and time-domain interpolation technique, the power efficiency of the proposed ADC can be improved by 42% compared to the DA-based flash ADC. The measured differential non-linearity (DNL) and integral non-linearity (INL) are -0.29/+0.17 LSB and -0.00/+0.30 LSB, respectively. The measured spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) at Nyquist input frequency are 36.63 dB and 24.21 dB, respectively, with a power consumption of 91 mW, and the figure of merit (FoM) is 172.6 pJ/conversion-step.**

***Keywords*— Analog-to-digital converter; complementary dynamic amplifier; interpolating flash ADC.**

Manuscript received 11 Jun. 2024; revised 14 Sep. 2024; accepted 7 Nov. 2024. Date of publication 31 Dec. 2024.

I. INTRODUCTION

Recently, various ADC architectures have been studied for a wide range of applications [1]-[12]. Among them, the Flash ADCs are primarily used in high-speed applications, such as wired and wireless communications [13]-[25]. However, a conventional n-bit flash ADC requires 2^n-1 comparators. As the resolution increases, the number of comparators grows rapidly, leading to increased input capacitance, area, and power consumption [26]. To address these drawbacks, several papers have proposed the use of interpolation techniques [27]-[28]. By employing the interpolation technique, additional zero-crossing points can be created between the outputs of neighboring comparators by connecting each comparator's output to a latch. This approach allows for the creation of zero-crossing points without the need for additional comparators, and as the interpolation factor increases, the number of required comparators decreases [29]. Consequently, reducing the number of comparators leads to a decrease in input capacitance, area, and power consumption, which are disadvantages of flash ADCs. However, the design challenges remain at the front end of the circuit. In previous studies, flash ADC structures that replace DA with CDA have been proposed to alleviate the burden of preamplifiers, which account for a large proportion of power consumption in flash ADCs [30]-[31]. While the DA performs the conversion at the rising edge of the clock by discharging two output nodes to the ground (GND) to amplify the input voltage difference and by charging them to the supply voltage (VDD) for the reset operation at the falling edge, the CDA performs both conversions and reset simultaneously at both the rising and falling edges. Therefore, CDA can operate at half the clock speed of DA, reducing the design burden on the clock driver. Additionally, since CDA outputs through two separate paths on the rising and falling edges, each path requires latches, and these latches operate in an interleaved manner, alleviating the burden of high-speed latch design. Although such CDA-based flash ADCs can alleviate power consumption and the burden of high-speed design, the design burden of the large number of comparators required in flash ADC structures remains.

This paper proposes a 4-bit 40 MS/s CDA-based 2-times time-domain interpolating flash ADC architecture.

In the proposed design, thanks to the application of CDA in the interpolating flash ADC, the interpolation technique benefits by reducing the number of comparators, input capacitance, area, and power consumption while alleviating the design burden on the clock driver and high-speed latch. Furthermore, a circuit was implemented to prevent inter-conversion interference in the SR-Latches caused by the operational characteristics of CDA.

II. Materials and Method

Fig. 1 shows the block diagram of the proposed 4-bit 40 MS/s CDA-based 2-times time-domain interpolating flash ADC. This ADC consists of 8 track-and-hold (T/H) circuits to generate different input voltages for each CDA, 8 CDAs to convert the sampled input voltage into time information, 15 NOR and NAND SR-latches (SRLs) modified to prevent unnecessary latching, multiplexers (MUXs) to combine the thermometer codes generated with each conversion, one 4-bit Wallace encoder for decoding the 15 thermometer codes into 4-bit binary codes, and an R-string for generating the reference voltages for the CDAs. The R-string generates eight reference voltages, and the T/H circuits take the input and reference voltages as inputs, passing the difference between the input and reference voltages (VHP, VHM) to the CDA. The CDA operates over two sampling cycles, converting voltage information into time information at both the rising and falling edges of the operating clock. The proposed SR-latch converts This information into digital information (thermometer code). Due to the operational characteristics of the CDA, both NAND and NOR SRLs are required. Since these operate interleaved, a MUX transfers the signals to the encoder. Finally, the thermometer code is converted into a 4-bit binary code by the 4-bit Wallace encoder. This configuration enables the implementation of a 4-bit 40MS/s CDA-based 2-times time-domain interpolating flash ADC with improved power efficiency compared to conventional flash ADCs.

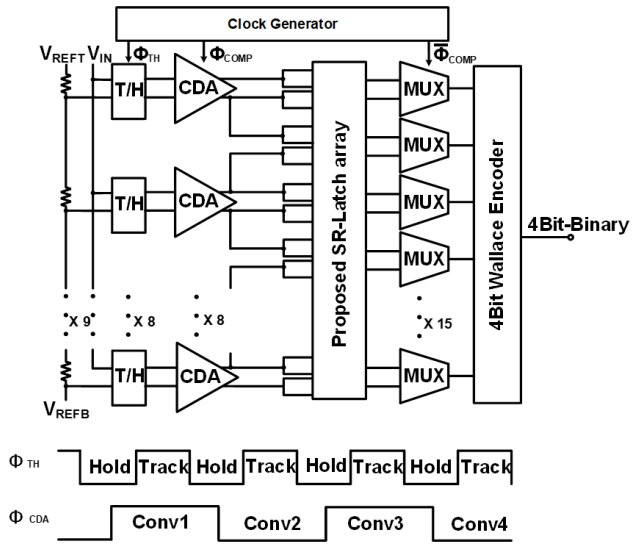

Fig. 1 Block diagram

A. Complementary Dynamic Amplifier

Fig. 2 illustrates the operation of DA and CDA. As shown in Fig. 2 (a), at the rising edge of the Φ_{DA}, PMOS transistors M3 and M4 turn off, while NMOS transistors M5 and M6 turn on. The two outputs (V_{SN} and V_{SP}) discharge to VSS at a rate proportional to the magnitude of the inputs (V_{HP} and V_{HM}) at M7 and M8(Conv mode).

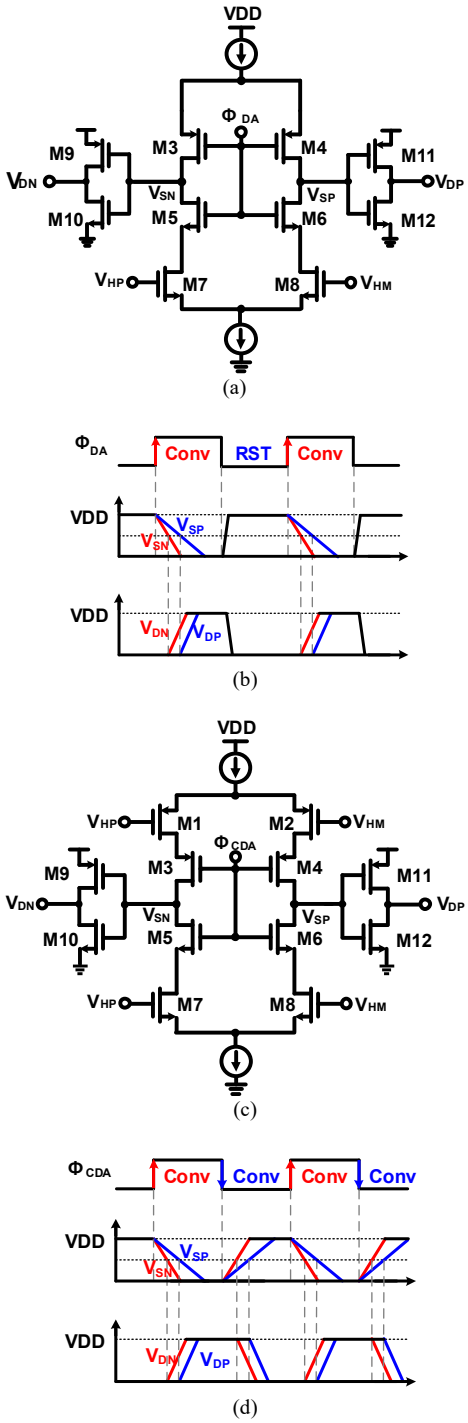

Fig. 2 Timing diagram of dynamic amplifiers (a) DA (b) timing diagram of DA (c) CDA (d) timing diagram of CDA

If V_{HP} is greater than V_{HM}, V_{SN} discharges faster than V_{SP}, as shown in Fig. 2 (b). After passing through inverters composed of M9, M10, M11, and M12, V_{DN} and V_{DP} exhibit a time difference corresponding to the slope difference

between V_{SN} and V_{SP}. At the falling edge of the Φ_{DA}, both outputs (V_{SP} and V_{SN}) are reset to VDD in preparation for the subsequent conversion (RST mode). On the other hand, as shown in Fig. 2 (b), at the rising edge of the Φ_{CDA}, V_{SN}, and V_{SP} discharge to VSS at a rate proportional to the magnitude of the inputs (V_{HP} and V_{HM}) at M7 and M8(Conv), similar to DA. If V_{HP} is greater than V_{HM}, V_{SN} discharges faster than V_{SP}, as illustrated in Fig. 2 (b). After passing through inverters composed of M9, M10, M11, and M12, V_{DN} and V_{DP} exhibit a time difference corresponding to the slope difference between V_{SN} and V_{SP}. CDA's two outputs (V_{SP} and V_{SN}) complete discharging to VSS (conversion + reset) before the next falling edge. At the falling edge of the Φ_{CDA}, the two outputs are charged to VDD at a rate proportional to the magnitude of the inputs (V_{HP} and V_{HM}) at M1 and M2. If V_{HP} is smaller than V_{HM}, then V_{SN} charges faster than V_{SP} (Conv). After passing through inverters composed of M9, M10, M11, and M12, V_{DN} and V_{DP} exhibit a time difference corresponding to the slope difference between V_{SN} and V_{SP}. Before the rising edge of the Φ_{CDA}, both outputs (V_{SP} and V_{SN}) complete charging to VDD (reset to VDD). In other words, because CDA can perform two conversions within one clock cycle, it can operate at half the clock speed of the DA, and by reusing the reset current offers better power efficiency. Fig. 3 shows the simulation results comparing the current consumption of a DA array and a CDA array in 2-times time-domain interpolating flash ADC.

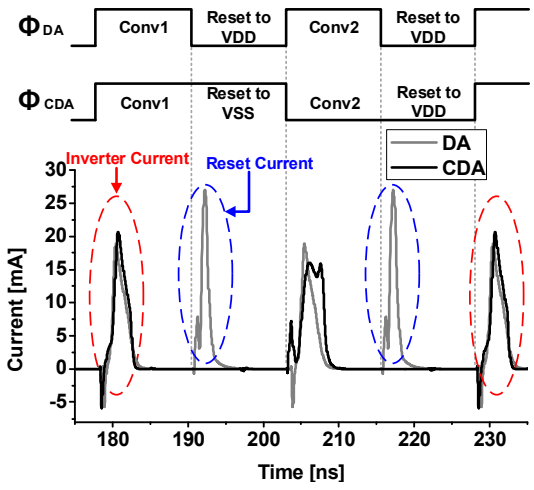

Fig. 3 Simulation result for comparing current consumption of DA and CDA

In [4], the reset currents of DA and CDA were compared using a 40 nm CMOS process. In this paper, the comparison is conducted using a 500 nm CMOS process. The current consumption occurring at the rising edge of the clock for both CDA and DA is due to the inverters connected to their outputs, as shown in Fig. 2(c). This current is consumed when the output of the inverters charges to VDD, and it occurs in both DA and CDA. On the other hand, DA performs the conversion operation at the rising edge of Φ_{DA} and resets to VDD at the falling edge of Φ_{DA}, resulting in a current spike being observed in every cycle. In contrast, CDA performs conversion 1 (Conv 1) and then resets to VSS. After performing conversion 2 (Conv 2) at the falling edge of Φ_{CDA}, it resets to VDD. As a result, reset current spikes are not observed in CDA because the reset current is reused for the next conversion. By applying CDA, which has better power efficiency and operates at half the clock speed compared to DA, the power efficiency of the ADC has been improved. The improved power efficiency will be discussed further in Table I.

B. Interpolating Technique

A flash ADC with interpolation techniques has advantages such as reduced input capacitance, smaller area, and improved power efficiency due to the reduced number of comparators. Additionally, an interpolating flash ADC reduces the burden of offset calibration between comparators [1]. In this paper, we applied a 2-times time-domain interpolation technique, and Fig. 4 is a simplified illustration of the interpolating unit cell.

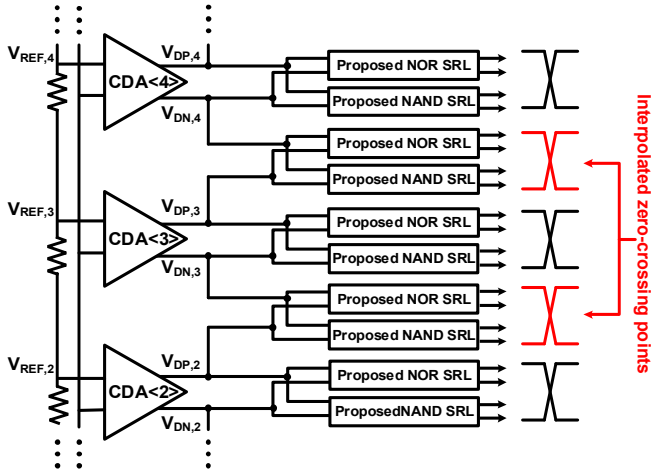

Fig. 4 Simplified interpolation unit cell

To generate additional zero-crossing (ZX) points between two neighboring CDAs, the outputs of each CDA are connected to SR latches. The explanation aims to detail the interpolation technique used with the CDA's output through Fig. 5. Fig. 5 (a) shows the output of the CDA when the input magnitude is greater than $V_{REF,3}$ but less than $\frac{V_{REF,3} + V_{REF,4}}{2}$. In this case, $V_{SP,3}$ discharges faster than $V_{SN,4}$, and $V_{DP,3}$ rises first, followed by $V_{DN,4}$. As the input gradually increases, $V_{SP,3}$ discharges more slowly, while $V_{SN,4}$ discharges faster. In Fig. 5 (b), when $V_{in} = \frac{V_{REF,3} + V_{REF,4}}{2}$, $V_{SP,3}$ and $V_{SN,4}$ have the same slope, and $V_{DP,3}$ and $V_{DN,4}$ rise simultaneously. In Fig. 5 (c), when the input exceeds $\frac{V_{REF,3} + V_{REF,4}}{2}$, $V_{SN,4}$ discharges faster than $V_{SP,3}$, causing $V_{DN,4}$ to rise first, followed by $V_{DP,3}$. At this point, the output of the latch connected to $V_{DN,4}$ and $V_{DP,3}$ changes from Q = 0, QB = 1 to Q = 1, QB = 0. The operation of the latches will be explained in Section III–C. By applying the 2-times time-domain interpolation technique, 15 zero-crossing points can be generated using just 8 CDAs. As shown in Table 1, this interpolation technique improved power consumption by approximately 42.3% compared to a DA-based full flash architecture.

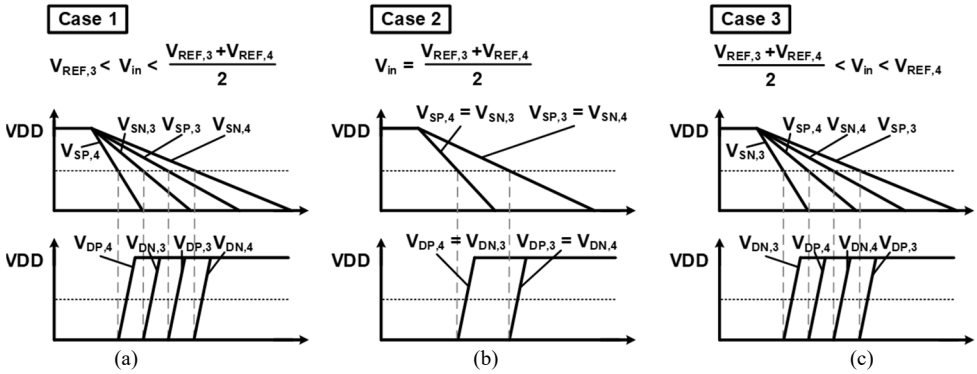

Fig. 5 Transient waveforms of CDA in Fig. 4 (a) case 1 (b) case 2 (c) case 3

C. Proposed SR-Latches

Fig. 6 (a) shows the conventional NOR SR-latch, and Fig. 6 (b) shows the proposed NOR SR-latch. [32] presents an architecture with a CDA applied to an Asynchronous Loop-Unrolled [LU] SAR-Flash hybrid ADC. Inter-conversion interference was observed in the NOR latch when the CDA was connected to the latch. As shown in Fig. 6 (c), the NOR-latch receives $S(V_{DP}) = 0$ and $R(V_{DN}) = 1$ (falling edge of Φ_{CDA}), maintaining $Q = 0$ and $QB = 1$. If the rise of V_{DP} occurs first, followed by V_{DN} (rising edge of the Φ_{CDA}), and the NOR latch receives $S(V_{DP}) = 1$ and $R(V_{DN}) = 0$, unwanted latching occurs due to the NOR function of the latch.

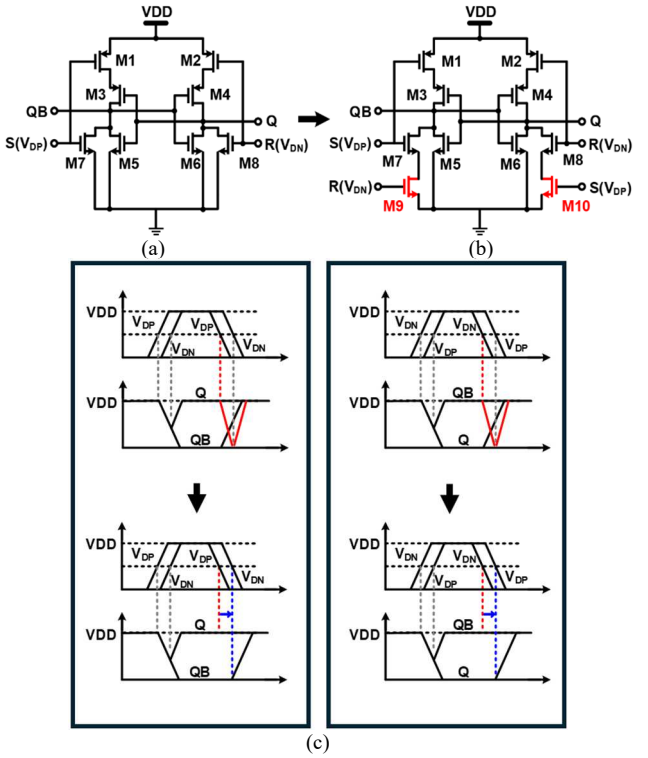

Fig. 6 Operation of proposed NOR SR-Latch (a) conventional NOR SR-Latch (b) proposed NOR SR-Latch (c) timing diagram

Similarly, when $S(V_{DP}) = 1$ and $R(V_{DN}) = 0$ are input, the latch maintains $Q = 1$ and $QB = 0$. If V_{DN} rises first, followed by V_{DP}, unwanted latching occurs again. This inter-conversion interference was a factor that degraded the ADC's performance. Transistors M9 and M10 were added to prevent this issue, as shown in Fig. 6 (b). Adding transistors M9 and M10 prevents unwanted latching even if V_{DP} or V_{DN} rises first, followed by the other input. However, in this paper, while inter-conversion interference does not degrade performance, the same method was applied to prevent unwanted latching in the SR latch. Since the CDA output has two directions (charging toward VDD and discharging toward VSS), NOR and NAND SR latches must be used. Inter-conversion interference was also observed in the NAND SR-latch used in this case. Fig. 7 (a) shows the conventional NAND SR-latch and Fig. 7 (b) shows the proposed NAND SR-latch. As shown in Fig. 7 (c), the NAND SR-latch receives inputs of $S(V_{DP}) = 1$ and $R(V_{DN}) = 0$ (rising edge of Φ_{CDA}), maintaining $Q = 1$ and $QB = 0$.

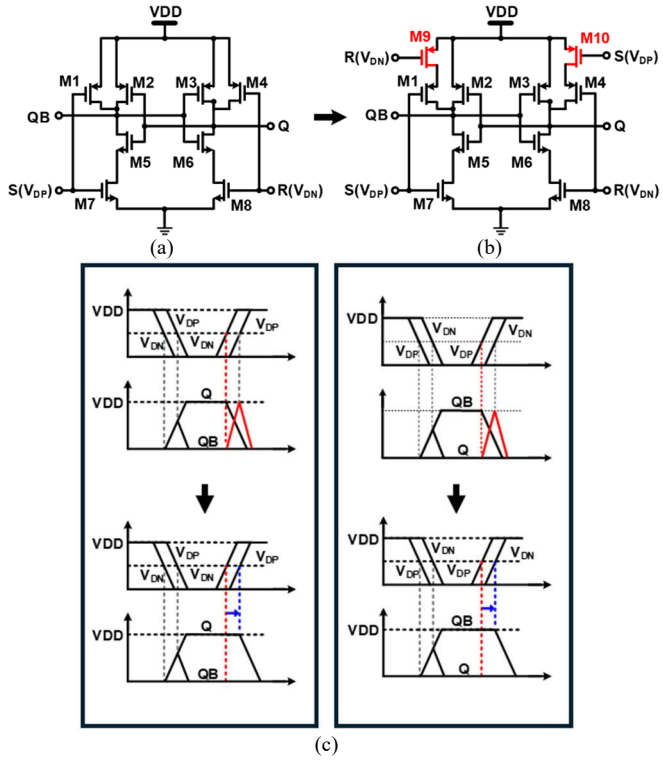

Fig. 7 Operation of proposed NAND SR-Latch (a) conventional NAND SR-Latch (b) proposed NAND SR-Latch (c) timing diagram

If V_{DP} falls first, followed by V_{DN} (falling edge of Φ_{CDA}), the NAND SR-latch's inputs become $S(V_{DP}) = 1$ and $R(V_{DN}) = 0$, leading to unwanted latching due to the NAND function of the latch. Similarly, when $S(V_{DP}) = 0$ and $R(V_{DN}) = 1$ are input, the latch maintains $Q = 0$ and $QB = 1$. If V_{DN} falls first,

followed by V_{DP}, unwanted latching occurs. Transistors M9 and M10 were added to prevent this interference, as shown in Fig. 7 (b). Adding M9 and M10 prevents unwanted latching even if V_{DP} or V_{DN} falls first and the other input follows.

Table I compares the power breakdown of three architectures under the conditions of a sampling frequency of 40 MS/s, input of 3.5 $V_{PP,DIFF}$ (VCM = 2.5), input frequency = 19.375 MHz (Nyquist input) and supply voltage of 5V: DA-based full-flash architecture without interpolation technique (DA-based flash), DA-based 2-times time domain interpolating flash ADC (DA-based IP flash), and CDA-based 2-times time domain interpolating flash ADC (CDA-based IP flash). In the DA-based flash, 15 T/H units and 15 DAs are used as the interpolation technique is not applied. As mentioned earlier, applying the interpolation technique reduces the required number of DAs, CDAs, and T/H units to 8, resulting in higher power consumption in the T/H and DA arrays in the DA-based flash compared to the DA-based IP flash architecture. The power consumption in the SRLs array shows a negligible difference of 0.1mW, and the power consumption in the encoder is similar.

TABLE I
POWER BREAKDOWN

	DA-based Flash	DA-based IP Flash	CDA-based IP Flash
DA or CDA array	22.13 mW	11.16 mW (49.6%)	7.26 mW (67.2%)
CLK driver	9.2 mW	7.92 mW (13.9%)	5.73 mW (37.7%)
Track-and Hold(T/H)	4.35 mW	2.28 mW (47.6%)	2.28 mW (47.6%)
SRLs array	1.5 mW	1.59 mW (-0.1%)	656.4 uW (56.2%)
Encoder	5.02 mW	5.18 mW (-3.2%)	5.99 mW (-19.3%)
R-string	2.92 mW	2.92 mW	2.92 mW
Total	43.05 mW	31.05 mW (27.9%)	24.84 mW (42.3%)

By applying the interpolation technique, power consumption in the T/H and DA array improved by 47.6% and 49.6%, respectively, with an overall power consumption improvement of 27.9%. When comparing the CDA-based IP flash and DA-based flash architectures, the power consumption in the T/H and CDA array was improved by 47.6 % and 67.2 %. And a 37.7 % improvement in the CLK driver. It was observed that the encoder consumed an additional 0.97 mW of power due to the MUX that was added to combine the outputs of the NOR SR-latch and the NAND SR-latch. The total power consumption improved by approximately 42.3%. In the CDA-based IP flash architecture, it was found that power consumption in the SRLs array was reduced compared to that in the DA-based IP flash architecture. This is because the DA's output alternates between conversion and reset in each cycle, which causes changes in the SR-Latch output, resulting in current consumption. This current consumption varies depending on the input frequency, as shown in Fig. 8, which illustrates the power consumption variation of the SR-latch array with varying input frequency.

As a result of sweeping the input frequency, it was confirmed that the SR-latch used in the DA-based IP flash ADC consumes more power near the Nyquist input, whereas the SR-latch used in the CDA-based IP ADC shows reduced power consumption. The operation speed of the latch array used in the DA is the same as the sampling frequency (fs). Therefore, the most enormous code transition occurs at 1/2 fs, causing the highest power consumption near the Nyquist input. On the other hand, the CDA performs conversions at each sampling frequency (fs), and as shown in Fig. 2(d), the output directions are opposite. Hence, as previously mentioned, NOR SR-latches and NAND SR-latches are required for each direction. The operation speed of the CDA latch is half the sampling frequency (i.e., $\frac{1}{2}f_S$).

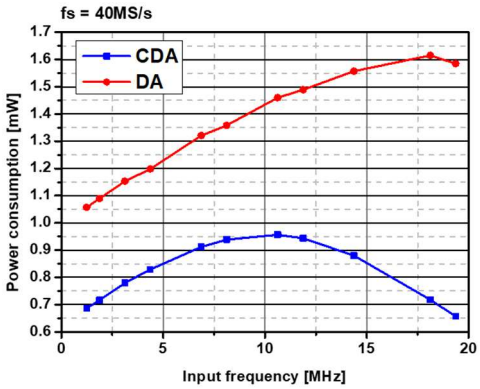

Fig. 8 Variation of power consumption of the SR-latch array

As a result, the most extensive code transition occurs at $\frac{1}{4}f_S$, and as shown in Fig. 8, power consumption is highest at $\frac{1}{4}f_S$. As the frequency approaches $\frac{1}{2}f_S$, the number of code transitions decreases, leading to a gradual reduction in power consumption. However, this variation in power consumption does not significantly affect the overall power consumption, as it constitutes a small portion.

III. RESULTS AND DISCUSSION

Fig. 9 is a photograph of a 4-bit 40 MS/s CDA-based 2-times time domain interpolating flash ADC fabricated using a 500nm CMOS process. It consists of a T/H circuit, R-string, CDA array, SRL array, and logic. The dimensions are 0.99mm by 0.99mm.

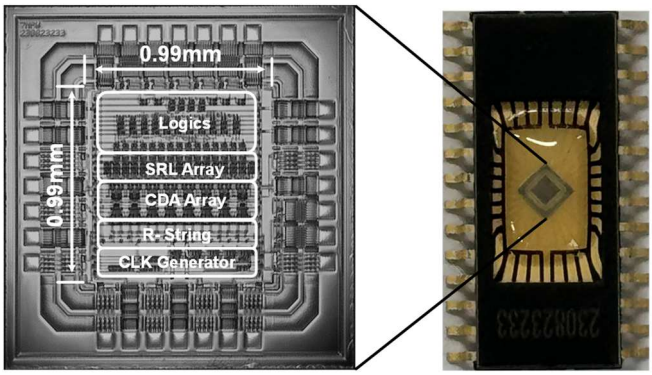

Fig. 9 Die photograph

Fig. 10 shows the measurement setup for the prototype ADC. The input signal is applied differentially through a balun, and the clock is applied as a single-channel signal. The ADC's digital code is transmitted to a PC for real-time performance evaluation.

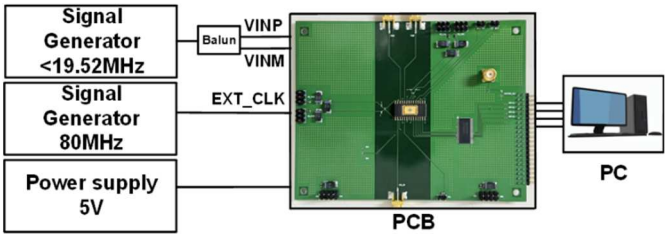

Fig. 10 Measurement setup

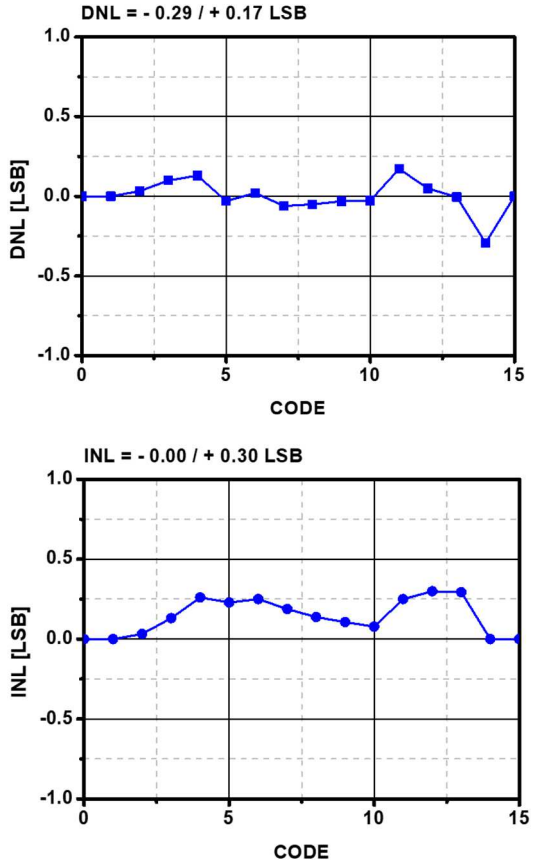

Fig. 11 Measured DNL and INL

Fig. 11 shows the measured Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). Even without mismatch calibration, the peak DNL and INL are -0.29 / +0.17 LSB and -0.00 / +0.30 LSB, respectively. Fig. 12 shows the measured FFT spectrum. With a sampling frequency of 40 MS/s and an input frequency of 721 KHz (Fig. 12 (a)), the measured spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are 35.02dB and 23.95dB (ENOB = 3.68 bits), respectively. At an input frequency of 19.52 MHz (Fig. 12 (b)), the measured SFDR and SNDR are 36.63dB and 24.21dB (ENOB = 3.72 bits). When the input frequency is 30.42 MHz (Fig. 12 (c)), the measured SFDR and SNDR are 36.31dB and 24.16dB (ENOB = 3.71 bits).

Fig. 13 (a) shows the performance variation according to the change in input frequency. It can be observed that the performance remains stable up to around 30 MHz, after which it gradually decreases. Fig. 13 (b) shows the performance variation with changes in sampling frequency. The performance remains stable up to 40 MS/s, but from 42 MS/s onward, the performance gradually decreases.

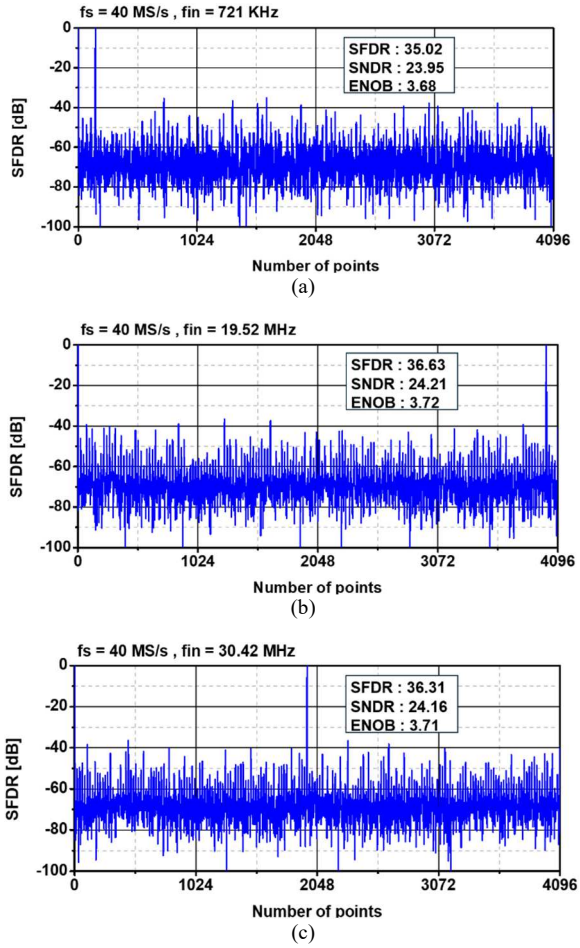

Fig. 12 Measured FFT spectrum according to the input frequencies with 40 MS/s of sampling frequency. (a) 721 KHz input (b) 19.52 MHz input (c) 30.42 MHz input.

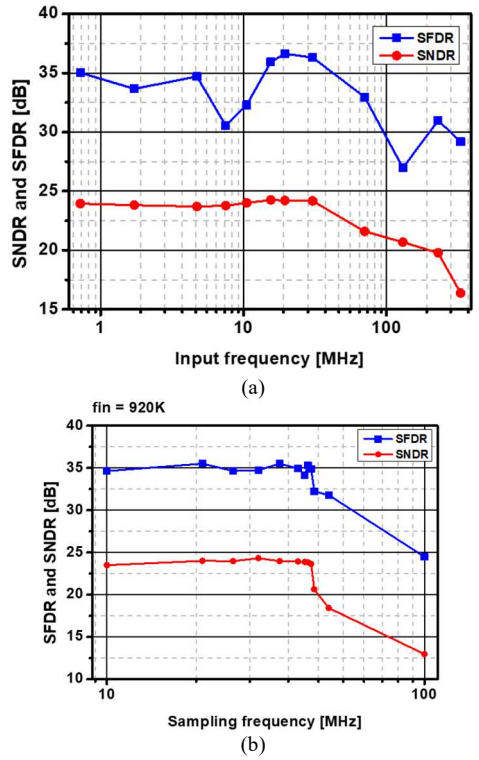

Fig. 13 Measured SNDR and SFDR (a) various input frequencies at 40 MS/s and (b) various sampling frequencies at 920KHz input.

IV. Conclusion

A 4-bit CDA-based 2-times time-domain interpolating flash ADC was presented using a 500-nm CMOS (2-poly, 3-metal) process. By employing interpolation techniques, the number of comparators required for the 4-bit flash ADC was reduced from 15 to 8, and CDA was used instead of the conventional DA for better power efficiency. The proposed SR latches were applied with CDA to eliminate inter-conversion interference. This led to reductions in area, input capacitance, and power consumption and decreased the burden of offset calibration between CDAs. Pre-layout simulation results comparing the power efficiency of the DA-based full flash ADC structure and the 4-bit CDA-based 2-times time-domain interpolating flash ADC showed an improvement of approximately 42.3% in power consumption. This figure reflects the additional power consumption due to dummy latches added to match the output loads of the CDA for MSB and LSB conversion and the MUX array used to combine the outputs of the two types of latches.

Measurement results of the prototype ADC revealed that with a supply voltage of 5V and at the Nyquist input, the SFDR is 36.63 dB, and the SNDR is 24.21 dB (ENOB = 3.72 bits). Due to the lack of offset and mismatch calibration between CDAs, some performance degradation is observed. The power consumption is 91 mW, and the figure of merit (FoM) is 172.6 pJ/conversion step.

Acknowledgment

This work was supported by the research grant of Jeju National University in 2023.

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