International Journal on
Advanced Science
Engineering
Information Technology

Vol. 2 (2012) No. 1
ISSN: 2088-5334

Design of Monolithic Integrator for Strain-to-Frequency Converter

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***Abstract*— Strain-to-Frequency converter (SFC) is a one of the analog conditioner tools that converts any strain signal to the frequency signal. The basic concept of SFC is by detecting any changing of strains, then converting the strain to the voltage signal and converting the voltage signal to the frequency signal. This tool consists of 3 main components which are strain gauge, differential integrator and comparator. This paper presents the designing and analysis of monolithic integrator that to be used in the Strain-to-Frequency converter. The primary goal is to design and simulate the performance of monolithic integrator for SFC using GATEWAY Silvaco Electronic Design Automation (S EDA) tools and EXPERT software. The performances of SFC using the designed monolithic integrator are also investigated.**

***Keywords*—Strain-to-Frequency converter(SFC); monolithic integrator; CMOS 0.18µm technology; GATEWAY Silvaco; EXPERT.**

I. INTRODUCTION

In SFC systems, one of key issues is designing of compact integrated circuit while providing high accuracy measurement. This paper presents the design of a compact monolithic integrator using the CMOS 0.18µm technology that to be implemented in SFC circuit. The circuit will be designed and simulated using GATEWAY software. Operational amplifier will be designed and analyzed first in order to obtain stable working condition. A few equations are used in determining the sizing of transistor for op amp stability [1].

$$GB = gm_2/Cc \quad (1)$$

$$Cc \geq 0.22C_L \quad (2)$$

$$gm_2 = \sqrt{2\beta_2 I_2} \quad (3)$$

$$\beta_2 = K'n_2 (W/L) \quad (4)$$

The designing and simulation process are continued for the integrator, strain gauge and comparator. A few expected values for the simulation will be setup first in achieving the accurate output result. After designing of all the components, each designed components will be combined in a complete Strain-to-frequency circuit. The SFC circuit will be simulated again in order to get the accurate output result as expected. Final step is designing the layout of monolithic integrator. The layout of monolithic integrator that was designed in GATEWAY will be drawn and checked using EXPERT software.

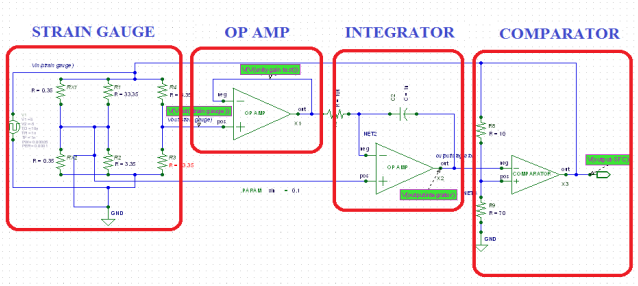

Fig. 1 Schematic of SFC

II. RESULTS AND DISCUSSION

The project consists of two major processes which are sketching the schematic of SFC and drawing the layout of monolithic integrator. The op amp is designed based on the specification. Table 1 shows the general critical parameter specifications for basic op amp.

To achieve all specified parameters, the circuit is analyzed using AC and transient analysis. Integrator will be designed using the designed op amp. The RC circuit with 1µF capacitor and 1MΩ resistor will be applied to the op amp. The signal output will be analyzed in the wide range For the Strain Gauge, the value of the output will be simulated to enof frequency to ensure the output met the expected value.

For less critical applications, an op amp without negative feedback (open loop) is often used as a comparator [2]. In general, comparator cannot be used as op amp, but op amp

can be used as comparator in noncritical applications. Finally, the layout of the monolithic integrator is drawn using EXPERT software. The sketched schematic of op amp in GATEWAY will be linked to EXPERT software to ensure the accuracy of design.

TABLE I
SPECIFICATIONS FOR BASIC OP-AMP

Specifications	**Design Requirement**
Phase Margin	> 60˚
Unity Gain Frequency	> 5MHz
DC Gain	>100 (40dB)
Voltage Swings	1.0V to 4.0 V
Slew Rate	> 5V/µs

A. Design of Op- Amp

As very high gain bandwidth product will make the op amp to be unstable [3]. The value of width and length has been adjusted to control the amount of current in a transistor in making more stability of op amp. Table 2 shows the simulation results for the op amp and clearly shows that the op-amp has met the specifications.

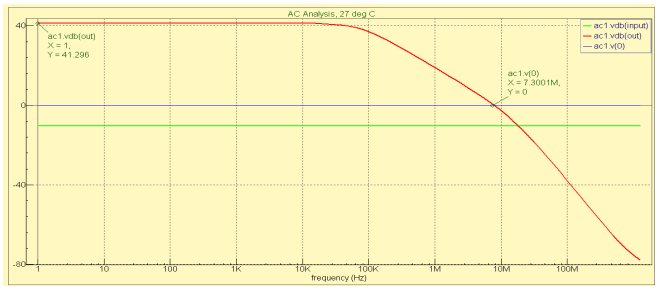

Fig. 2 AC analysis

TABLE 2
THE OP-AMP SIMULATION RESULT

Specifications	Expected	Results
Phase Margin	60˚	89˚
Unity Gain Frequency	5MHz	7.3MHz
DC Gain	100 (40dB)	116.1 (41.296dB)
Slew Rate	5V/µs	13.91V/µs

B. Design and Simulation of Integrator

As the capacitor charges or discharges, a current flow through capacitor is totally restricted by the internal resistance of the capacitor. This internal resistance is known as capacitive reactance which varies with frequency. As the frequency applied to the capacitor increases the reactance decreases and vice versa [4].

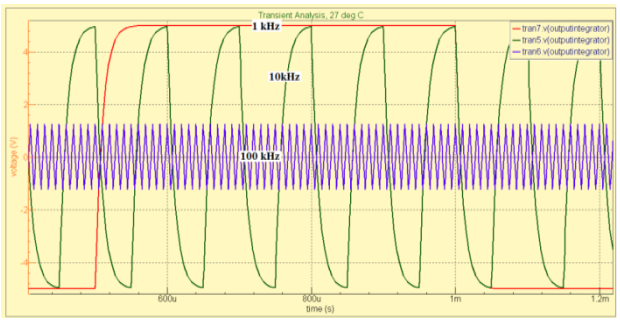

Fig. 3 Combination output of integrator

C. Design and simulation of Strain Gauge

The circuit in simulation result is happening after 3Ω fractional of strain occurs.

The output is 4.5843V and met the targeted value, thus this schematic will be used in SFC schematic later.

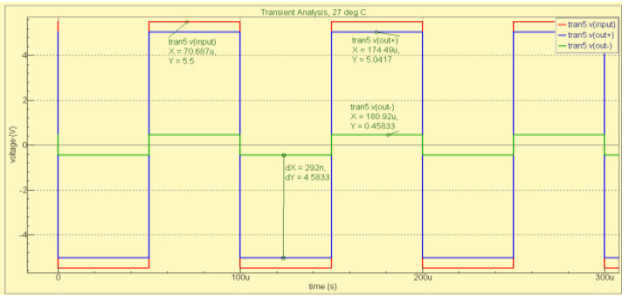

Fig. 4 Output of strain gauge

D. Design and simulation of Comparator

When the output is at the maximum positive voltage and the input exceeds UTP (upper trigger point), the output holds about 10 microseconds and switches to the maximum negative voltage. When the output is at the maximum negative voltage and the input exceeds LTP (lower trigger point), the output holds about 10 microseconds and switches to the maximum positive voltage. The holding output at 10 microseconds is caused by input signal frequency complete the circle at 20 microseconds for complementary input step cycle.

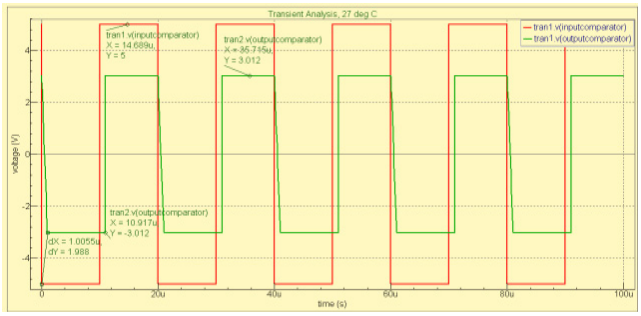

Fig. 5 Output of comparator

E. Design and simulation of SFC

The source of strain gauge is 3.5V and producing 2.9V out of balance from the bridge resistor. The output of integrator is 3.7V while the output of SFC is 2.18V. To calculate the frequency, consider the circuit is starting at time is zero. If fractional occurs in strain gauge, the out of

balance is produced and become input for voltage divider at comparator stage. At time is zero, there is no output from the integrator, but there are output from comparator. The frequency of SFC is 50 kHz.

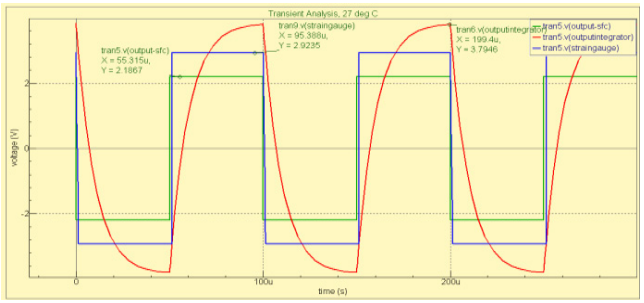

Fig. 6: Output of SFC simulation

F. Layout of monolithic integrator

The layoutof integrators consists of 5 NMOSs, 3 PMOSs, 2 capacitors and a resitor meanwhile the layout of op-amp has 9 transistors and a compensator. The negative input is connected to the resistor and capacitor. The capacitor is connected in feedback of output of integrator. The positive input is grounded to the ground. The complete layout of monolithic integrator as shown in Fig. 7 is drawn with size of 42µm length and 25µm width.

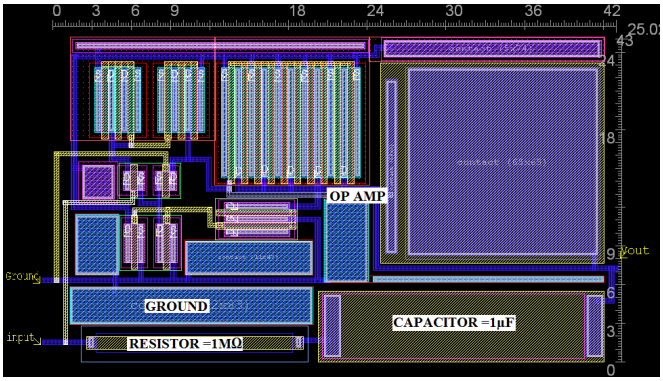

Fig. 7: Monolithic Integrator layout

III. CONCLUSIONS

The layout of the compact monolithic integrator is produced using EXPERT with the size is 1.05mm^2.This layout which comprises op- amp, 1uF capacitor and also 1MΩ resistor is verified using DRC and LVS. Based on the results obatained, the simulation output is met the targeted specifications as the high slew op-amp to produce more stable operation.

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